AMENDMENTS TO THE CLAIMS

Please amend claim 13, as shown below.

The following is a complete list of all claims in this application.

1-12. (Cancelled)

13. (Currently Amended) A method for manufacturing a thin film transistor (TFT) array panel, comprising steps of:

depositing a first conductive layer formed of aluminum or aluminum alloy material on a substrate;

patterning the first conductive layer to form a gate line and a gate pad connected to the gate line;

depositing an insulating layer on the gate line and the gate pad;

forming a semiconductor layer on the insulating layer;

depositing a second conductive layer on the semiconductor layer;

patterning the second conductive layer to form a data line;

forming a contact hole extending through the insulating layer and exposing the aluminum or aluminum alloy material of the gate pad;

<u>performing an annealing process;</u>

depositing using a sputtering process a third conductive layer formed of an indium zinc oxide (IZO) layer; and

patterning the third conductive layer to form a conductive pattern directly contacting the aluminum or aluminum alloy material of the gate pad in the contact hole, wherein the

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sputtering process is performed at a temperature below 200° C, wherein the annealing process is performed immediately before depositing the third conductive layer.

14-15. (Cancelled)

16. (Previously Amended) The method of claim 13, wherein the step of depositing the third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO.

17. (Previously Presented) The method of claim 16, wherein a content rate of Zn in the compound is between about 15% and about 20%.

18. (Previously Amended) The method of claim 13, wherein the step of patterning the third conductive layer comprises a step of forming a pixel electrode connected to the data line.

19. (Previously Amended) A method for manufacturing a thin film transistor array panel, comprising steps of:

depositing a first conductive layer formed of aluminum or aluminum alloy material on a substrate;

patterning the first conductive layer to form a gate line, a gate electrode and a gate pad;

depositing a gate insulating layer;

forming a semiconductor layer on the gate insulating layer;

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depositing a second conductive layer over the gate insulating layer and the semiconductor layer;

patterning the second conductive layer to form a data line, a source electrode and a drain electrode;

forming a passivation layer over the gate insulating layer and the data line;

forming a contact hole extending through the passivation layer and the gate insulating layer and exposing the aluminum or aluminum alloy material of the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer over the passivation layer; and

patterning the third conductive layer to form a redundant gate pad directly contacting the aluminum or aluminum alloy material of the gate pad through the contact hole.

20. (Previously Amended) The method of claim 19, wherein the step of patterning the third conductive layer comprises a step of patterning the third conductive layer to form a pixel electrode.

21. (Previously Amended) The method of claim 19, wherein the step of patterning the second conductive layer comprises a step of patterning the second conductive layer to form a data pad, and

the step of patterning the third conductive layer comprises a step of patterning the third conductive layer to form a redundant data pad connected to the data pad.

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22. (Previously Presented) The method of claim 19, wherein the step of forming the passivation layer comprises a step of depositing a silicon nitride layer at a temperature between about 280° C and about 400° C.

23. (Cancelled)

24. (Previously Amended) The method of claim 19, wherein the step of depositing the third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO.

25. (Previously Presented) The method of claim 24, wherein a content rate of Zn in the compound is between about 15% and about 20%.

26. (Previously Amended) The method of claim 19, wherein the step of patterning the second conductive layer comprises a step of patterning the semiconductor layer and the second conductive layer simultaneously by using a photoresist pattern having portions with different thicknesses.

27. (Previously Presented) The method of claim 26, wherein the photoresist pattern comprises a first portion having a first thickness, a second portion having a second thickness greater than the first thickness, and a third portion having a third thickness smaller than the first thickness.

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28. (Previously Presented) The method of claim 27, wherein a mask used for forming the photoresist pattern has a first area having a first transmittance, a second area having a second transmittance smaller than the first transmittance, and a third area having a third transmittance greater than the first transmittance.

29. (Previously Amended) The method of claim 28, wherein the first portion of the photo resist pattern is aligned on a portion between the source electrode and the drain electrode, and the second portion of the photoresist pattern is aligned on the data line .

30. (Previously Presented) The method of claim 29, wherein the first area of the mask includes a partially transparent layer or a pattern reducing a transmittance.

31. (Previously Presented) The method of claim 30, wherein the first thickness is less than a half of the second thickness.

32. (Previously Amended) The method of claim 31, further comprising a step of depositing an ohmic contact layer between the source and drain electrodes and the semiconductor layer.

33. (Previously Amended) The method of claim 32, wherein the second_conductive layer, the ohmic contact layer, and the semiconductor layer are patterned by a single photolithography process.

34-43. (Cancelled)

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44. (Previously Amended) A method for manufacturing a thin film transistor (TFT) array panel, comprising steps of:

depositing a first conductive layer formed of aluminum or aluminum alloy material on a substrate;

patterning the first conductive layer to form a gate line and a gate pad connected to the gate line;

depositing an insulating layer on a gate line and the gate pad;

forming a semiconductor layer on the insulating layer;

depositing a second conductive layer on the semiconductor layers;

patterning the second conductive layer to form a data line;

forming a contact hole extending through insulating the layer and exposing the aluminum or aluminum alloy material of the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer; and

patterning the third conductive layer to form a conduction pattern directly contacting the aluminum or aluminum alloy material of the gate pad in the contact hole, further comprising, preheating the passivation layer, the silicon nitride layer and the exposed gate pad before the forming the third conductive layer.

45-46. (Cancelled)

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47. (Previously Presented) The method of claim 13, wherein the insulating layer is comprised of silicon nitride.

48. (Previously Presented) the method of claim 47, wherein the insulating layer of silicon nitride is deposited at a temperature between about 280° C and about 400 ° C.

49. (Previously Presented) The method of claim 13, wherein a thickness of the IZO layer is about 500Å.

50. (Previously Presented) The method of claim 19, wherein depositing a gate insulating layer comprises depositing a layer of silicon nitride.

51. (Previously Presented) The method of claim 13, wherein the insulating layer is comprised of silicon nitride.

52. (Previously Presented) The method of claim 51, wherein the insulating layer is deposited at a temperature between about 280°C and about 400°C.

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